

### Claims

What is claimed is:

- 1 1. A memory system, comprising:
  - 2 a programmable storage device to store one or more indicators;
  - 3 cache tag logic; and
  - 4 a control circuit coupled to the storage device and to the cache tag logic, the
  - 5 control circuit to receive data and to determine, based on the one or more indicators,
  - 6 whether to update the cache tag logic to track the data.
- 1 2. The memory system of Claim 1, and further including a cache coupled to the
  - 2 cache tag logic to store the data, and wherein the control circuit further includes
  - 3 circuits to determine, based on the one or more indicators, whether to store the data
  - 4 to the cache.
- 1 3. The memory system of Claim 2, wherein one of the indicators indicates the
  - 2 cache is not available for use.
- 1 4. The memory system of Claim 2, and further including:
  - 2 at least one requester coupled to the control circuit to request data from, and
  - 3 store data to, the cache;

4           a main memory to provide to the cache requested data that is not stored  
5   within the cache; and  
6           wherein the control circuit includes a circuit that may replace the data in the  
7   cache based on the state of the indicators.

1   5.     The memory system of Claim 4, wherein the main memory provides data to  
2   the cache in response to a request that is any one of multiple request types, wherein  
3   at least one of the indicators identifies one or more of the request types, and wherein  
4   the control circuit prevents the replacement of the data in the cache if the data was  
5   provided in response to any of the identified request types.

1   6.     The memory system of Claim 4, wherein the one or more request types  
2   includes a request type indicating the data will be modified by a requester.

1   7.     The memory system of Claim 4, wherein at least one of the indicators  
2   identifies one or more of the at least one requester, and wherein the control circuit  
3   replaces the data in the cache if the data was returned from the main memory in  
4   response to a request issued by any of the identified requesters.

1   8.     The memory system of Claim 4, wherein the main memory provides data to  
2   the cache with a response that is any one of multiple response types, wherein at  
3   least one of the indicators identifies one or more of the response types, and wherein

4 the control circuit replaces the data in the cache if the data is returned from the main  
5 memory with any of the identified response types

1 9. The memory system of Claim 2, and further including at least one requester  
2 coupled to the control circuit to return data to the cache tag logic, and wherein the  
3 control circuit determines whether to store the returned data to the cache based on  
4 the state of at least one of the indicators.

1 10. The memory system of Claim 9, wherein the at least one requester returns  
2 data to the cache tag logic during an operation that is any one of multiple operation  
3 types, wherein the indicators include an indicator to identify one or more of the  
4 operation types, and wherein the control circuit stores the returned data to the cache  
5 if the returned data is returned during any of the identified operation types

1 11. The memory system of Claim 10, wherein the control circuit is further adapted  
2 to store the returned data to the cache based, at least in part, on whether a cache hit  
3 occurred.

1 12. The memory system of Claim 9, and further including a main memory coupled  
2 to the control circuit, and wherein the control circuit is adapted to forward the  
3 returned data to the main memory based, at least in part, on the state of at least one  
4 of the indicators.

1    13.    The memory system of Claim 12, wherein memory coherency actions may be  
2    incomplete for the returned data or for associated data retained by the at least one  
3    requester or the cache, and further including a request tracking circuit coupled to the  
4    control circuit to prevent the returned data from being forwarded to the main memory  
5    until all of the memory coherency actions have been completed for the returned data  
6    or for the associated data.

1    14.    The memory system of Claim 1, wherein the programmable storage device  
2    includes circuits to store microcode, and wherein the control circuit is controlled by  
3    the microcode..

1    15.    The method of Claim 1, and further including mode switch logic coupled to the  
2    programmable storage device to automatically re-program at least one of the  
3    indicators in response to monitored conditions occurring within the memory system.

1    16.    A method of controlling a memory system having cache tags and one or more  
2    programmable control indicators, comprising:  
3        a.) obtaining data; and  
4        b.) determining whether to update the cache tags to record the data based on  
5    the state of one or more of the control indicators.

1 17. The method of Claim 16, wherein the memory system includes a cache, and  
2 further including determining whether to store the data in the cache based on the  
3 state of one or more of the control indicators.

1 18. The method of Claim 17, wherein the memory system includes a main  
2 memory coupled to the cache tags, and wherein the obtaining step includes:  
3 providing a request for the data to the main memory; and  
4 receiving the data from the main memory.

1 19. The method of Claim 18, wherein the request is any one of multiple types,  
2 wherein one of the control indicators identifies one or more of the multiple request  
3 types, and wherein at least one of the determining steps is performed based, at least  
4 in part, upon whether the request is any of the identified response types.

1 20. The method of Claim 18, wherein the data is provided from the main memory  
2 with a response type that is any one of multiple response types, wherein one of the  
3 control indicators identifies one or more of the multiple response types, and wherein  
4 at least one of the determining steps is performed based, at least in part, upon  
5 whether the request is any of the identified response types.

1 21. The method of Claim 18, wherein the memory system is coupled to at least  
2 one requester, wherein one of the control indicators identifies one or more of the at  
3 least one requester, and wherein at least one of the determining steps is performed

4 based, at least in part, upon whether the request was initiated by any of the  
5 identified requesters.

1 22. The method of Claim 17, wherein the memory system is coupled to at least  
2 one requester, and wherein step a.) includes obtaining the data from any one of the  
3 at least one requester.

1 23. The method of Claim 22, wherein the data is obtained during an operation  
2 that is any of multiple operation types, wherein one of the control indicators identifies  
3 one or more of the operation types, and wherein at least one of the determining  
4 steps is based, at least in part, on whether the data is obtained during any of the  
5 identified operation types.

1 24. The method of Claim 23, wherein at least one of the determining steps is  
2 based, at least in part, on whether a cache hit occurs.

1 25. The method of Claim 22, wherein the memory system includes a main  
2 memory, and further including providing the data to the main memory instead of  
3 storing the data into the cache.

1 26. The method of Claim 25, wherein the data is associated with incomplete  
2 memory coherency actions, and further including preventing the data from being

3 provided to the main memory until all incomplete memory coherency actions have  
4 been completed.

1 27. The method of Claim 16, and further comprising:  
2 c.) monitoring conditions within the memory system; and  
3 d.) automatically re-programming at least one of the control indicators based  
4 on one or more of the monitored conditions.

1 28. A memory system, comprising:  
2 main memory means for storing data;  
3 cache means for storing a subset of the data; and  
4 programmable storage means for storing control indicators to select the  
5 subset of the data.

1 29. The memory system of Claim 28, wherein requests are issued to the main  
2 memory to retrieve data from the main memory, and wherein the programmable  
3 storage means includes means for selecting the subset of the data based, at least in  
4 part, on a type of request that was issued to retrieve the subset of the data from the  
5 main memory.

1 30. The memory system of Claim 28, and further including one or more requester  
2 means for causing data to be retrieved from the main memory, and wherein the  
3 programmable storage means includes means for selecting the subset of the data

4 based, at least in part, on the identify of one or more of the requester means that  
5 caused data to be retrieved from the main memory.

1 31. The memory system of Claim 28, wherein the main memory means includes  
2 means for returning a response type to the cache means with data, and wherein the  
3 programmable storage means includes means for selecting the subset of the data  
4 based, at least in part, on the response type.

1 32. The memory system of Claim 28, and further including requester means for  
2 returning data to the cache means, and wherein the programmable storage means  
3 includes means for selecting whether data returned by the requester means will be  
4 stored to the cache means.

1 33. The memory system of Claim 32, wherein the requester means includes  
2 means for returning data during any of multiple types of operations, and wherein the  
3 programmable storage means includes means for selecting whether returned data  
4 will be stored to the cache means based, at least in part, on the type of operation  
5 that resulted in return of the data.

1 34. The memory system of Claim 32, wherein the programmable storage means  
2 includes means for selecting whether data returned by the requester means will be  
3 stored to the cache means based, at least in part, on whether a cache miss occurred  
4 to the cache means.



1    35.    The memory system of Claim 28, and further including mode switch means  
2    for modifying the state of one or more of the control indicators based on monitored  
3    conditions occurring within the memory system.

1    36.    The memory system of Claim 28, and wherein the cache means includes  
2    cache tag means for tracking data that may be stored to the cache means, and  
3    wherein the programmable storage means includes means for determining whether  
4    to update the cache tag means to track data.

1    37.    The memory system of Claim 36, wherein the programmable storage means  
2    includes means for enabling the tracking by the cache tag means of predetermined  
3    data that is not included in the subset of the data stored within the cache means.